ECR #: 6
Title: Request followed by 2x write data with no turn-around
Release Date: Nov. 15, 1996
Impact: Clarification
Spec Version: A.G.P. 1.0

Summary:

A clarification is needed when describing 1x (requests) followed 2x (write data) with no turn-around cycle. Currently the electrical specification "appears" to have a conflict when this type of operation is done. A clarification is needed to draw attention to the designer that this is not a conflict in the spec but careful design consideration is required.

Background:

Figure 3-29 of the 1.0 specification illustrates this operation.

The actual numbers for understanding are:
0.5 (1x hold time) + 1.7 (2x data setup time to strobe) = 2.2. However, it is felt more appropriate for the designer to choose the min time to meet the 1x hold time and the 2x setup time.)

Change Current Specification as shown:

Add a sentence at the end of paragraph describing figure 3-29.

When this bus operation is supported by the master, careful review of the setup and hold times of the 1x and 2x timing parameters is warranted. See note 1 under table 4-4 A.G.P. 2X AC Timings Parameters for details.

Add Note 1 to Table 4-4

Note 1

When Write data immediately follows the enqueuing of requests (1x) (Figure 3-29) the min time of 2nsec causes a violation of the 1x hold time of the request. When this type of operation is supported by the master, the t_{TSf} min time is required to be greater than 2nsec.